WBS 6.5: Muon Phase II Upgrade

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University of Michigan

US ATLAS Phase II Managers Meeting
April 1st, 2015

Phase II Muon Upgrade in Brief

Baseline trigger requirements for Phase-II

- ➡ L0 trigger accept rate up to 1 MHz within 6 μs latency
- ➡ L1 trigger accept rate up to 400 kHz within 30 μs latency
- ➡ MDT data integrated into L1 trigger to sharpen muon p_T trigger

Requires the replacement of the front-end electronics for the MDT system

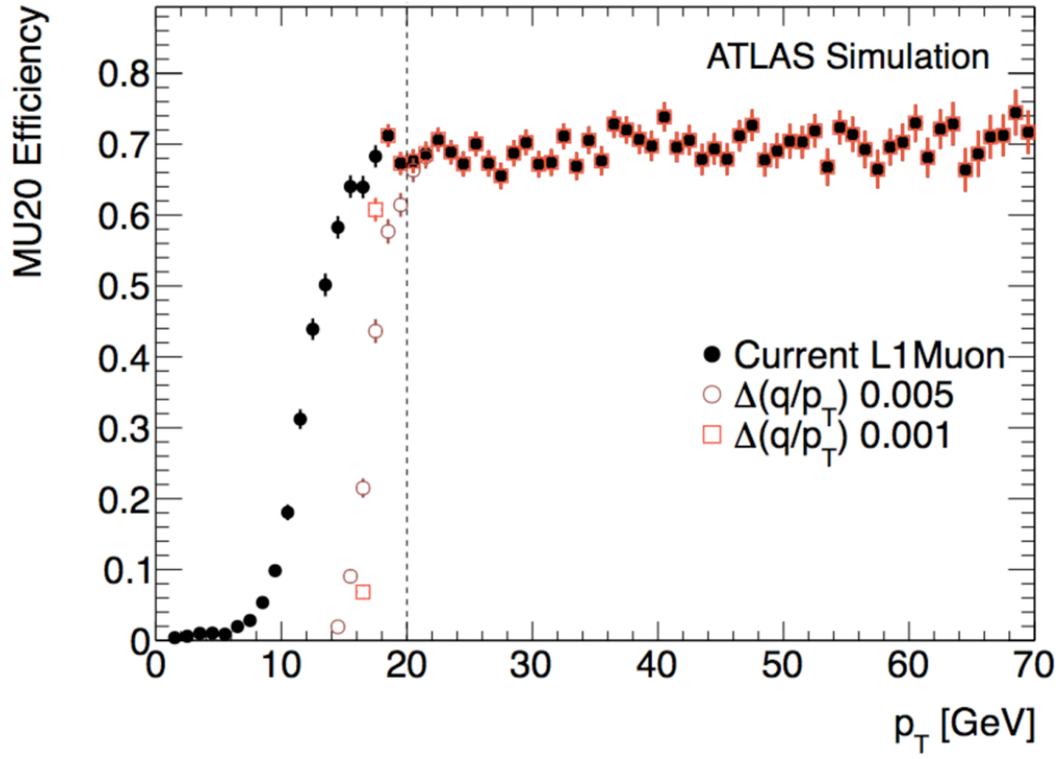
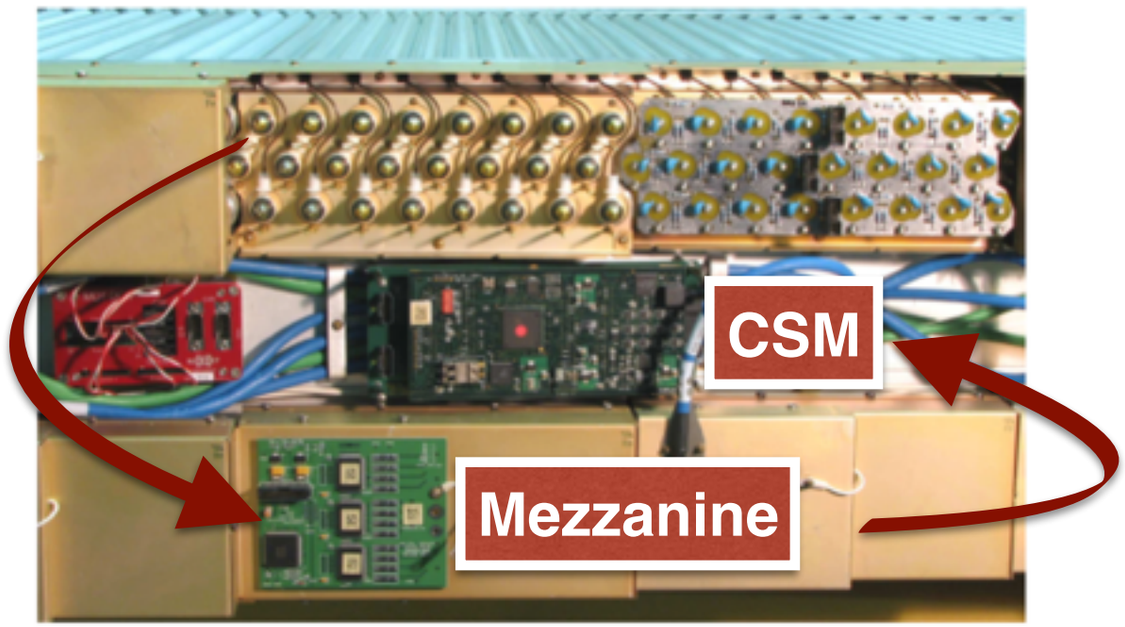


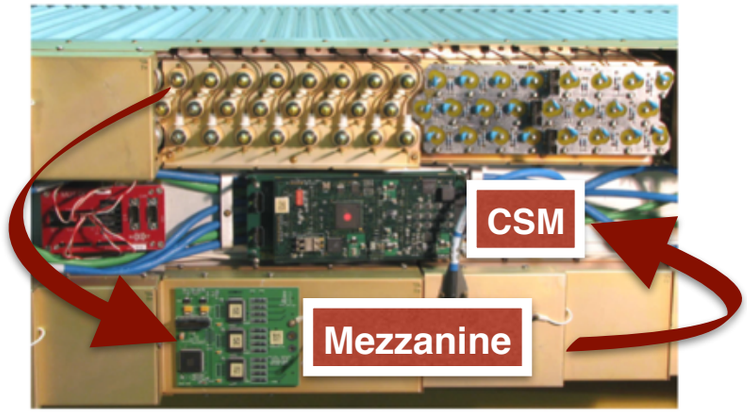
Figure 2: An open chamber of monitored drift tubes (MDT) after assembly.



Phase II Muon Upgrade in Brief

Mezzanine Card

➡ Consists of an ADC and TDC which performs sampling, time-stamping, and buffering of candidate Level 1 hits

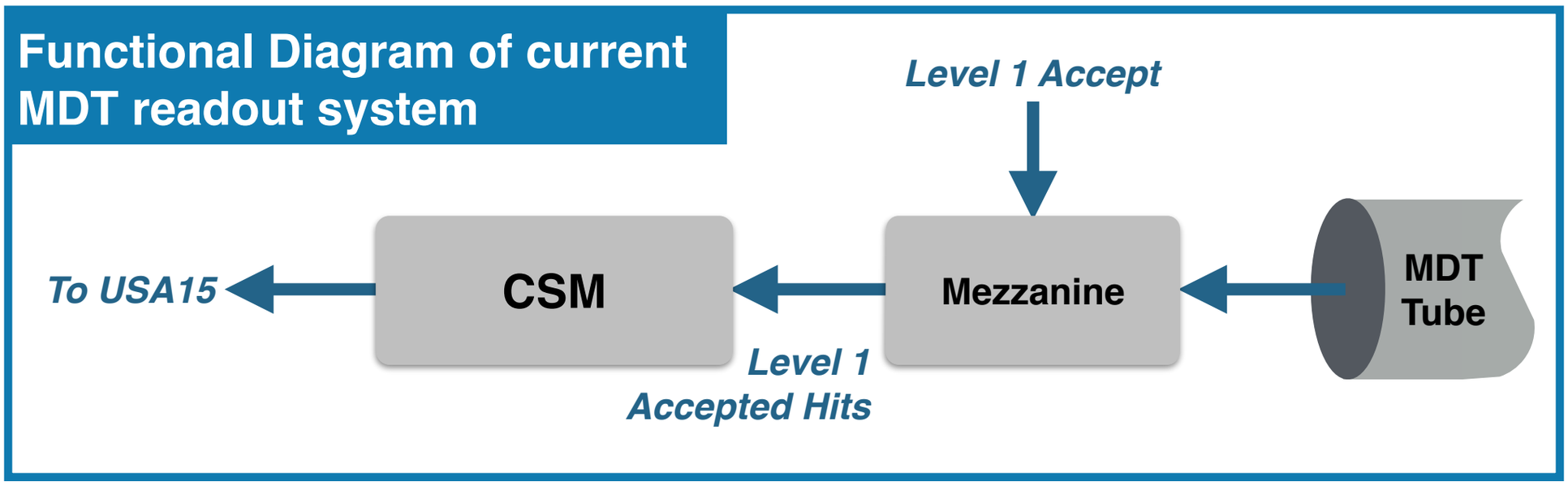


Chamber Service Module (CSM)

➡ Routes Level-1 accepted hits to readout at USA15

➡ Passes timing information to the TDC for time-stamping

➡ Handles control and monitoring

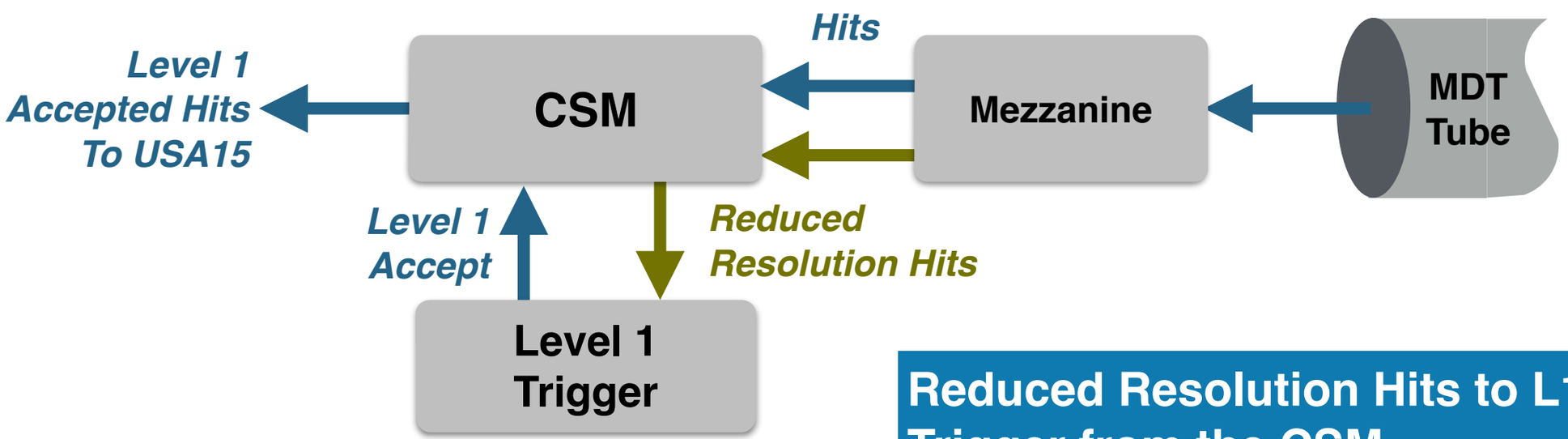


Phase II Muon Upgrade in Brief

Two requirements most affecting design

- ➡ L0 trigger accept rate up to 1 MHz within 6 μs latency
- ➡ MDT data integrated into L1 trigger to sharpen muon p_T trigger

Possible Design:



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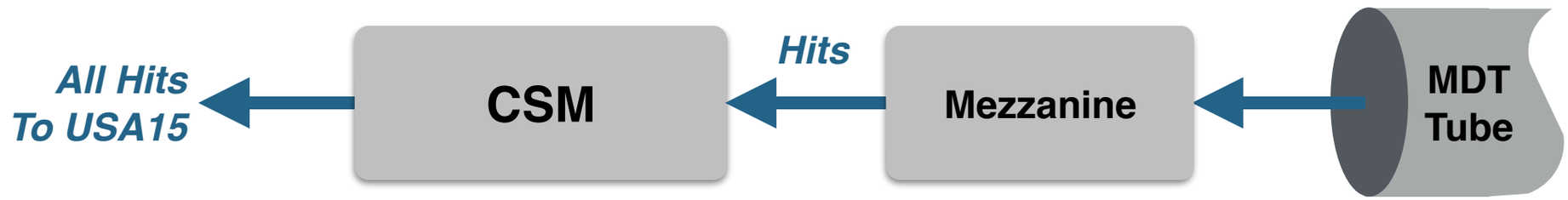
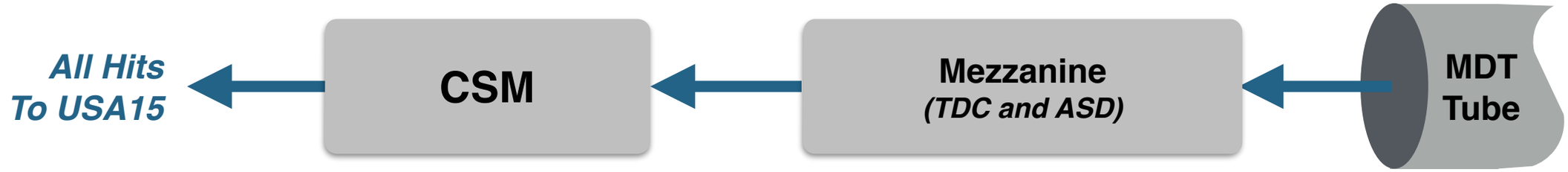


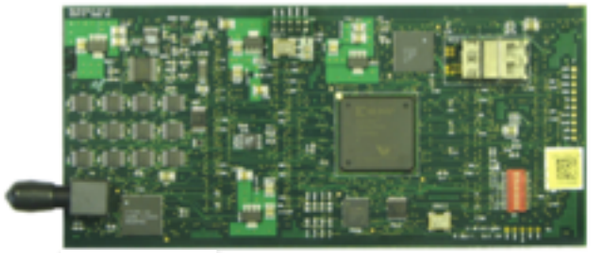
Full resolution hits to USA 15 (Trigger Processing) in time to be used for Level 1 ➜ 6 μs

US Deliverables for Phase II in Muons

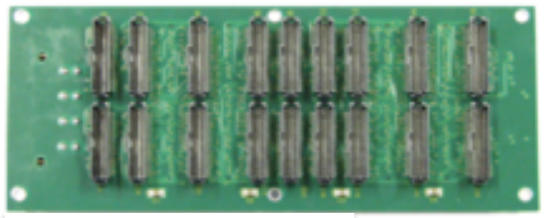
US Muons are late to the game, and so there's a great deal of uncertainty on what the FULL contribution will be - Below are possibilities



FPGA for Level-1 Matching

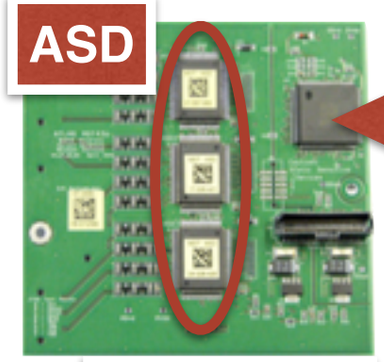


CSM



Motherboard

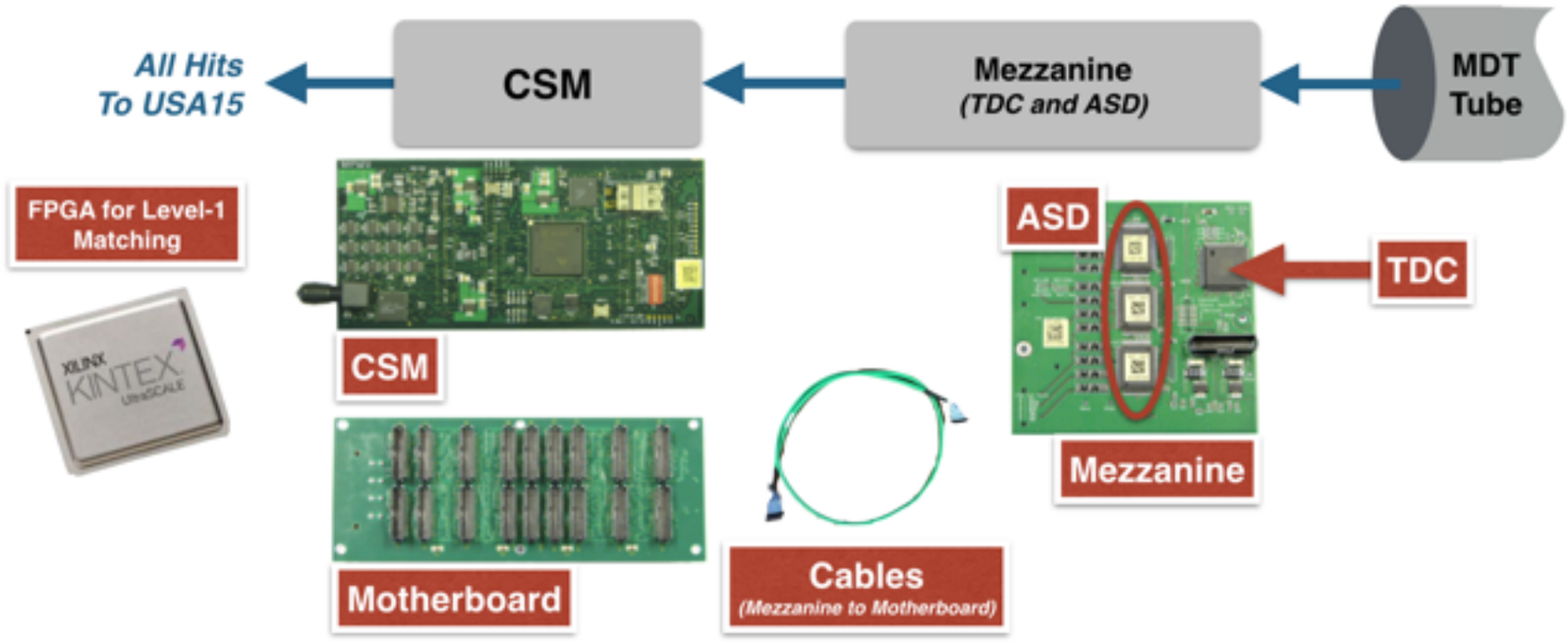
Cables
(Mezzanine to Motherboard)



Mezzanine

US Deliverables for Phase II in Muons

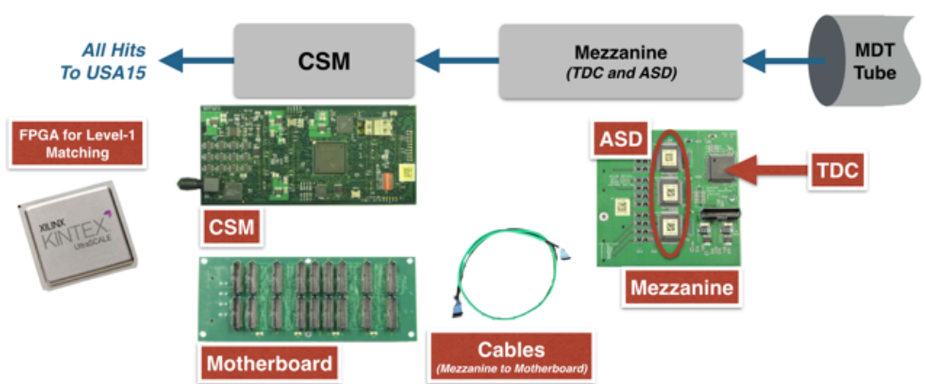
Deliverable
CSM Design/Construction
TDC Design/Construction
ASD Design/Construction
Mezzanine Design and Assembly
Motherboard/Cabling
FPGA to match hits for for Level 1 Trigger (@USA 15)



US Deliverables for Phase II in Muons

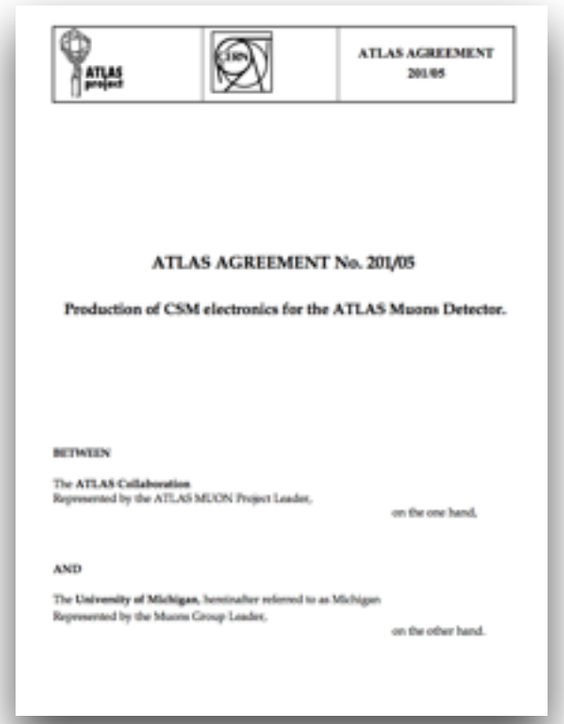
Deliverable	WBS #	US Institutions	Non-US	Funded US R&D	Construction Costs
CSM Design/Construction	6.5.1	Michigan		Yes	
TDC Design/Construction	6.5.2	BNL	CERN	sort of…	
ASD Design/Construction	6.5.3	BNL	MPI	sort of…	
Mezzanine Design and Assembly	6.5.4				
Motherboard/Cabling	6.5.5	Michigan? *I hope not…*		Yes	
FPGA to match hits for for Level 1 Trigger (@USA 15)	6.5.6		Japan?		

US Interests and Costs is current focus



CSM Construction Costs

- Starting point is a baseline Phase II design, including new FPGA and replacing some previous electronics with the GBT system of chips
- Assuming similar construction costs to the current ATLAS CSMs, accounting for new components, inflation, and exchange rates.
- Current CSM Construction costs taken from the 2003 ATLAS AGREEMENT 201-05 *"Production of CSM electronics for the ATLAS Muons Detector"*
- New Components, such as the GBT chips, are taken either from recent listed costs or from estimates of the developer/manufacturer (CERN for GBT)
- Fabrication, assembly and shipping costs per board for Phase II estimated from 201-05 w/ inflation applied
- Inflation Rates
  - ➡ 2003 - 2014 = 0.26
  - ➡ 2014 - 2021 assumed 0.03 per year
- Exchange Rate
  - ➡ 2003 = 0.74 CHF/USD
  - ➡ 2014 = 1.14 CHF/USD


ATLAS AGREEMENT
201/05

ATLAS AGREEMENT No. 201/05

Production of CSM electronics for the ATLAS Muons Detector.

BETWEEN

The ATLAS Collaboration
Represented by the ATLAS MUON Project Leader,
on the one hand,

AND

The University of Michigan, hereinafter referred to as Michigan
Represented by the Muons Group Leader,
on the other hand.

CSM Construction Costs

- There are currently 624 chambers in the barrel and 546 in the end cap, which require 608 and 510 CSM boards, respectively.
- NSW will not require CSM, so subtract 64 CSM
- New chambers (BME/BMR, BOE/BOR, BMG) require 22 additional CSM
- Assume 85% yield and 10% spares ➜ Go with same as 2003 = 1325

Components	Count	Cost / item
FPGA's	1325	$279.323
PROM's	1325	$15.802
GBLD, laser diode, housing	1325	$105.154
GBT-SCA	1325	$33.649
Misc Parts	1325	$175.015
GBTx	1325	$175.000
Fabrication and Assembly		$157.400
Total Cost per Board		$941

Basis of Estimate

Scaled costs from 2003

- Inflation Rates
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- Exchange Rate
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Basis of Estimate

- Scaled FGPA costs from 2003
- Additionally compared to costs of modern FPGA's in expected performance class

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Basis of Estimate

Current Cost Estimates Provided by CERN and scaled to 2021

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- Exchange Rate
  - ➡ 2014 = 1.14 CHF/USD

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1325 x $941 = $1.25M

CSM Construction Costs

		FY18		FY19		FY20		FY21		FY22	
		%	$ / hr	%	$ / hr	%	$ / hr	%	$ / hr	%	$ / hr
Personnel Effort and $/hr	Sr. Engineer	0.5	$93.48	1.0	$96.28	1.0	$99.17	1.0	$102.15	0.5	$105.21
	Jr. Engineer	0.5	$57.90	1.0	$59.64	1.0	$61.43	1.0	$63.27	0.5	$65.17
	Elec. Technician	0.5	$56.85	1.0	$58.56	1.0	$60.31	1.0	$62.12	0.5	$63.99
	Elec. Student	0.5	$35.48	1.0	$36.54	1.0	$37.64	1.0	$38.77	0.5	$39.93

Basis of Estimate

- Standard wages for personnel at Michigan with 3% yearly increase
- Expected personnel levels based on previous experience developing CSM at U-M

Previous CSM Development Team at U-M

- ➡ Jay Chapman (Sr Engineer equivalent) - CSM Leader/Firmware Design
- ➡ Pietro Binchi (Engineer) - Board design, left midway through development
- ➡ Bob Ball (Engineer) - CSM Firware, Board design, hired after Pietro left
- ➡ Tiesheng Dai (Engineer) - Test fixtures for MiniDAQ, test and debug
- ➡ Jon Ameel (Engineer) - Production, parts, testing on-site CERN
- ➡ Jeff Gregor and Tuan Anh Bui (Students) - Test and debug, some development

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Costs	Total Personnel Cost	$216,414	$445,814	$459,188	$472,964	$243,576
	Travel	$8,000	$8,000	$8,000	$8,000	$8,000
	Prototypes/Fixtures		$35,000	$20,000		
	Final Production				$1,250,000	
	Shipping				$35,000	
	Total Cost	$224,414	$488,814	$487,188	$1,765,964	$251,576
					Total	$3,217,957

w/out Contingency

Motherboards/Cabling Costs

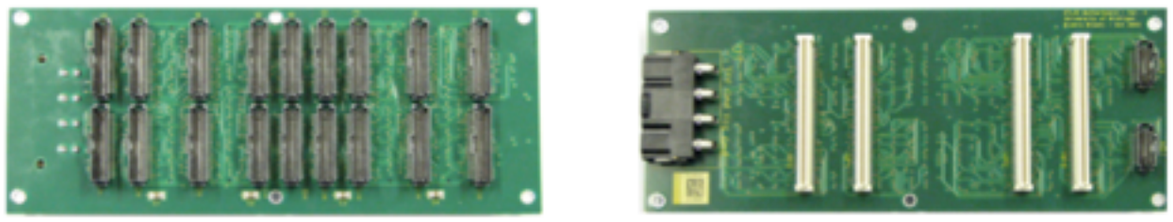
- Current CSM boards connected to mezzanine through a motherboard which re-routes the large # cables from the mezzanine to more compact pin connectors

  ➡ Not clear whether these cables/motherboards can handle the increased data rates for Phase-II

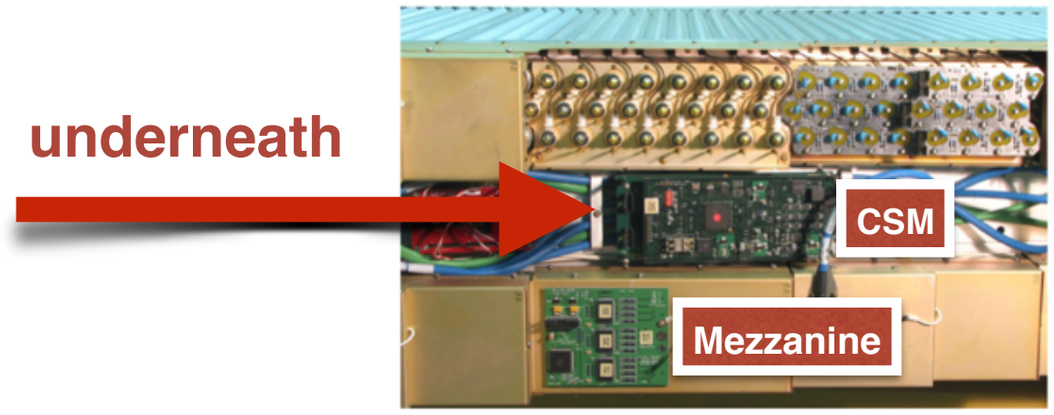
  ➡ Previously, motherboard was constructed in US ~ $120/board with inflation/contingency

  ➡ High-speed cables will range $15-30 (Halogen Free)

- Much bigger issue is additional labor and time to replace them!



Front and back of the motherboard which serves to connect the many cables from the front-end boards to more compact pin connectors which attach to the CSM.



Labor and Material Estimates by Dan Levin

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# Cables in Barrel	# Cables in Endcap (EM + EO)	Total	Contingency and Spares	$/cable	Total Cost
8054	*5648*	*13702*	*15000*	*17*	*$255K*

Number of Chambers	$/motherboard with connectors	Contingency 10%	Total Cost
1070	*$111*	*$121*	*$129K*

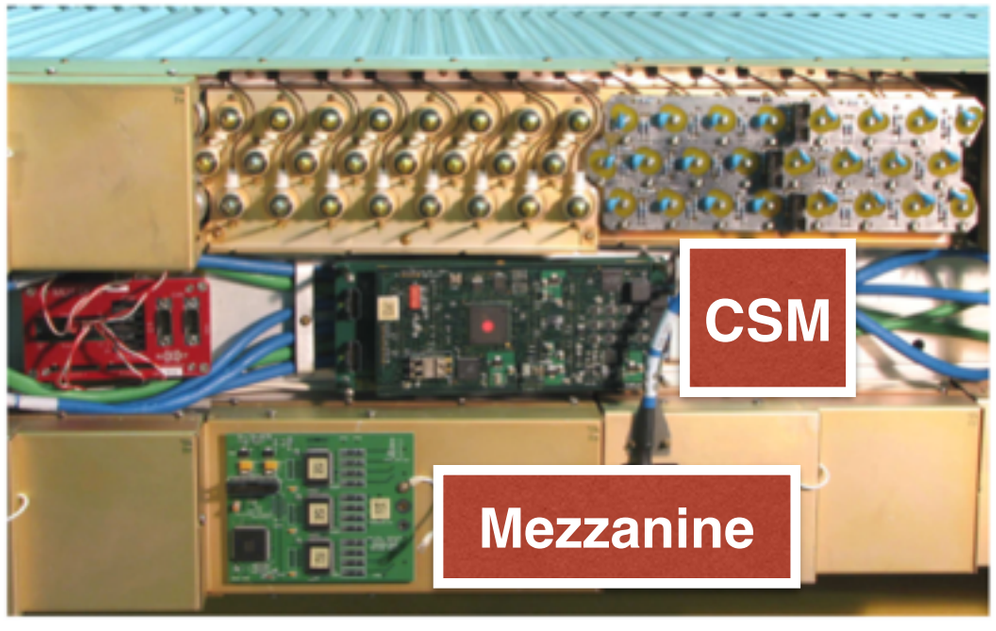
Labor and Material Estimates by Dan Levin

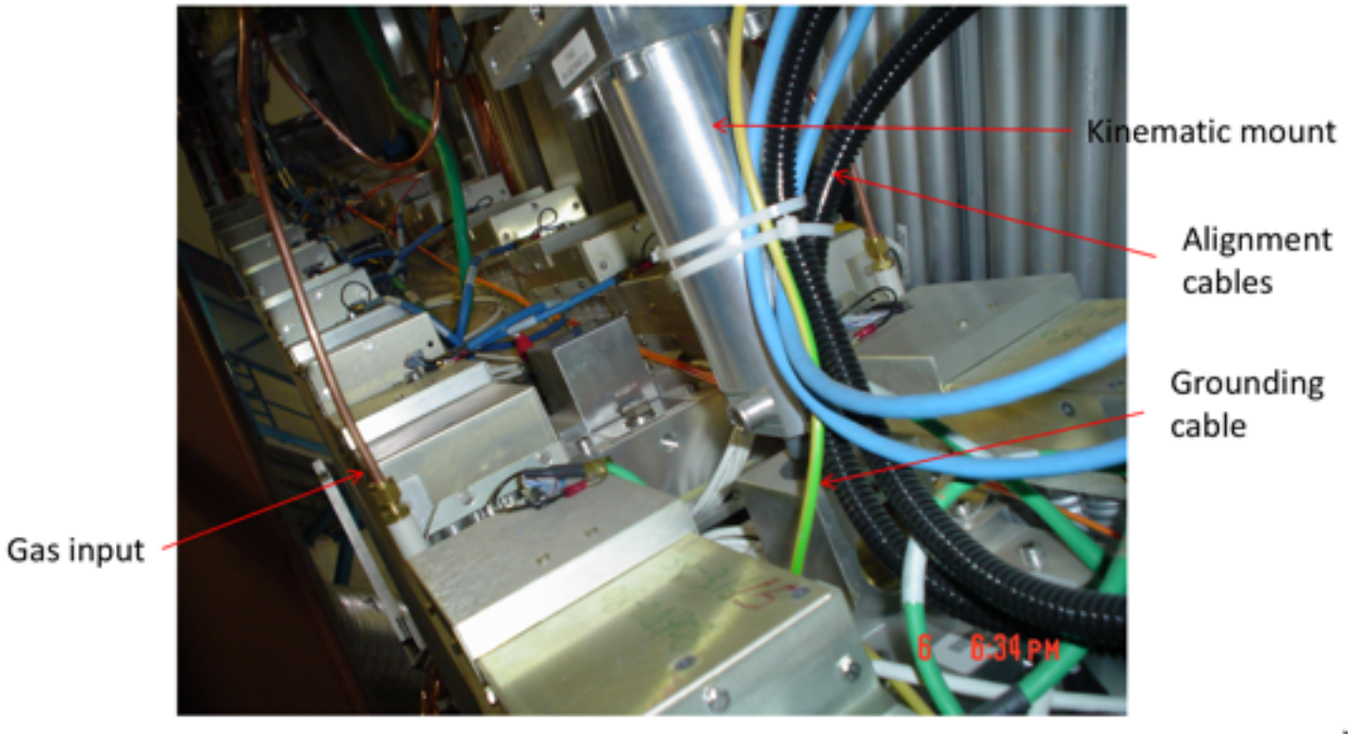
Motherboards/Cabling Labor Costs

- Not directly a US deliverable, but very much worth mentioning
- In-cavern Effort, assuming three sets of 2-person teams working 24 hrs

  ➡ Mezzanine and CSM replacement only (~ 40 min/chamber) ➜ Completed in 6.5 weeks

  ➡ Cable replacement (additional ~ 90 min/chamber) ➜ Completed in 21 weeks





Labor and Material Estimates by Dan Levin

Summary

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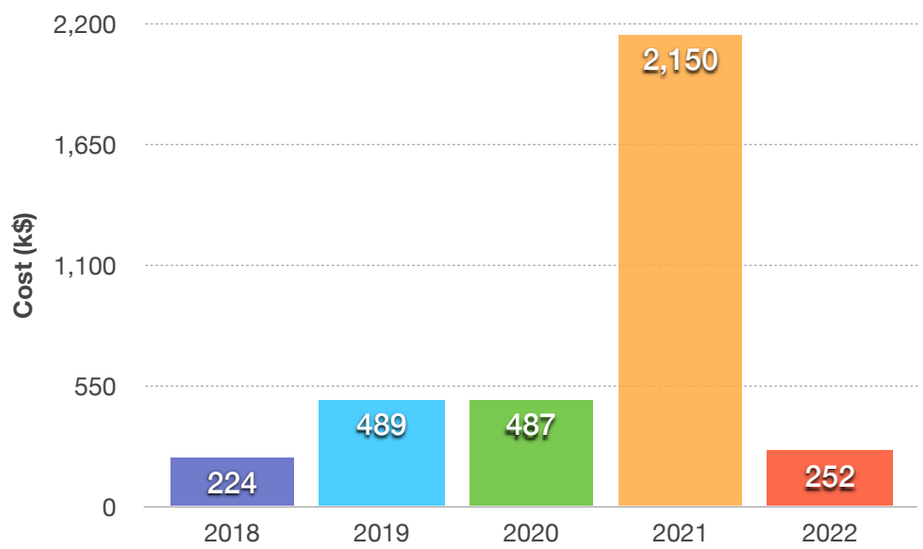
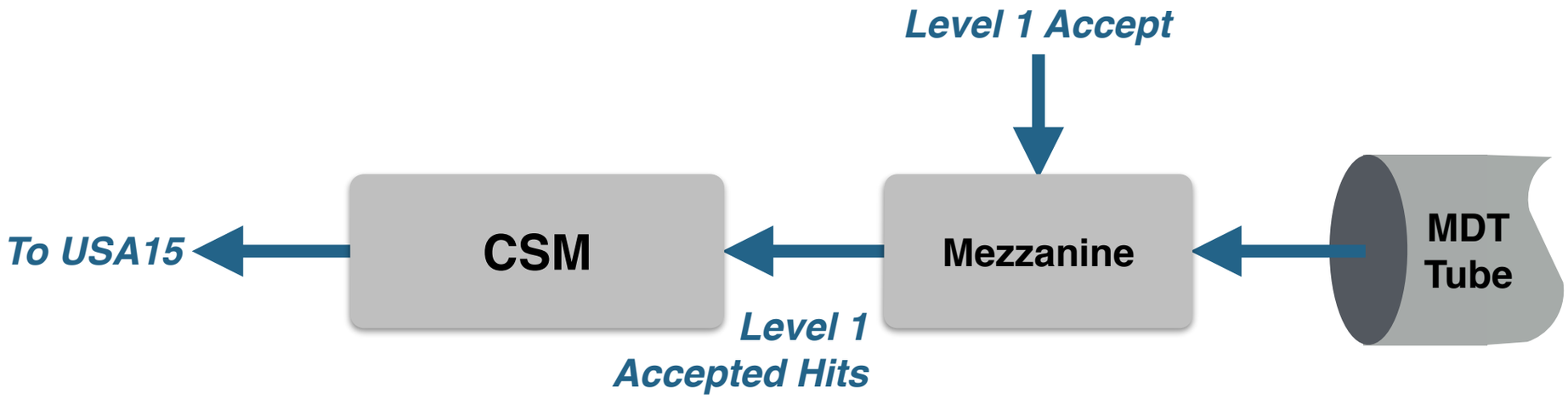
Mezzanine Design and Assembly	6.5.4				
Motherboard/Cabling	6.5.5	Michigan? *I hope not…*		Yes	$384k
FPGA to match hits for for Level 1 Trigger (@USA 15)	6.5.6		Japan?		

- Phase II interest is currently being fleshed out in US Muon community (NSW construction is dominating everyone's focus)
- Only "known" contribution is the CSM (costs have been estimated)
- As new Phase II R&D interest is gauged US deliverables will become clear

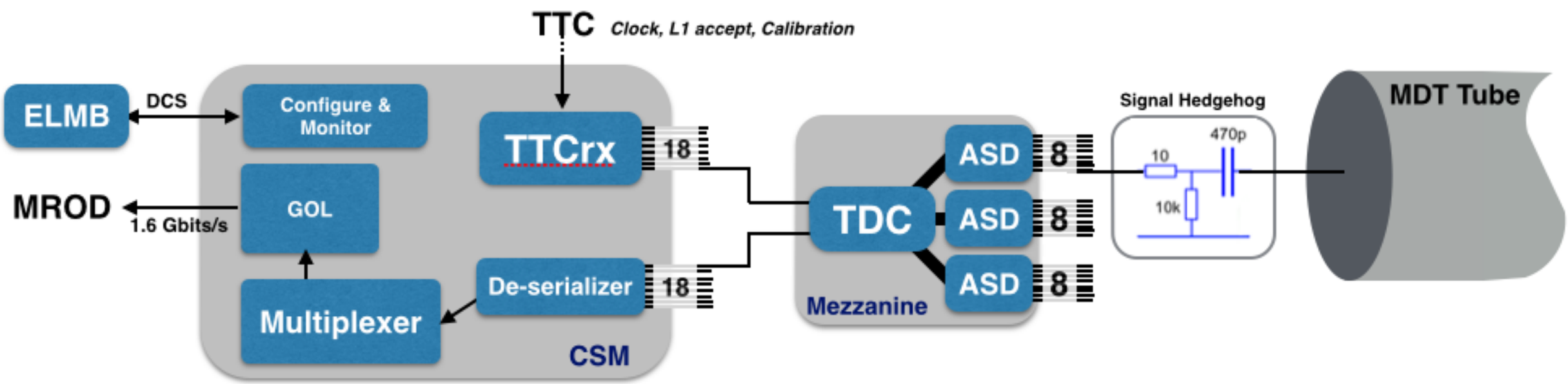


Backup

Phase II Muon Upgrade

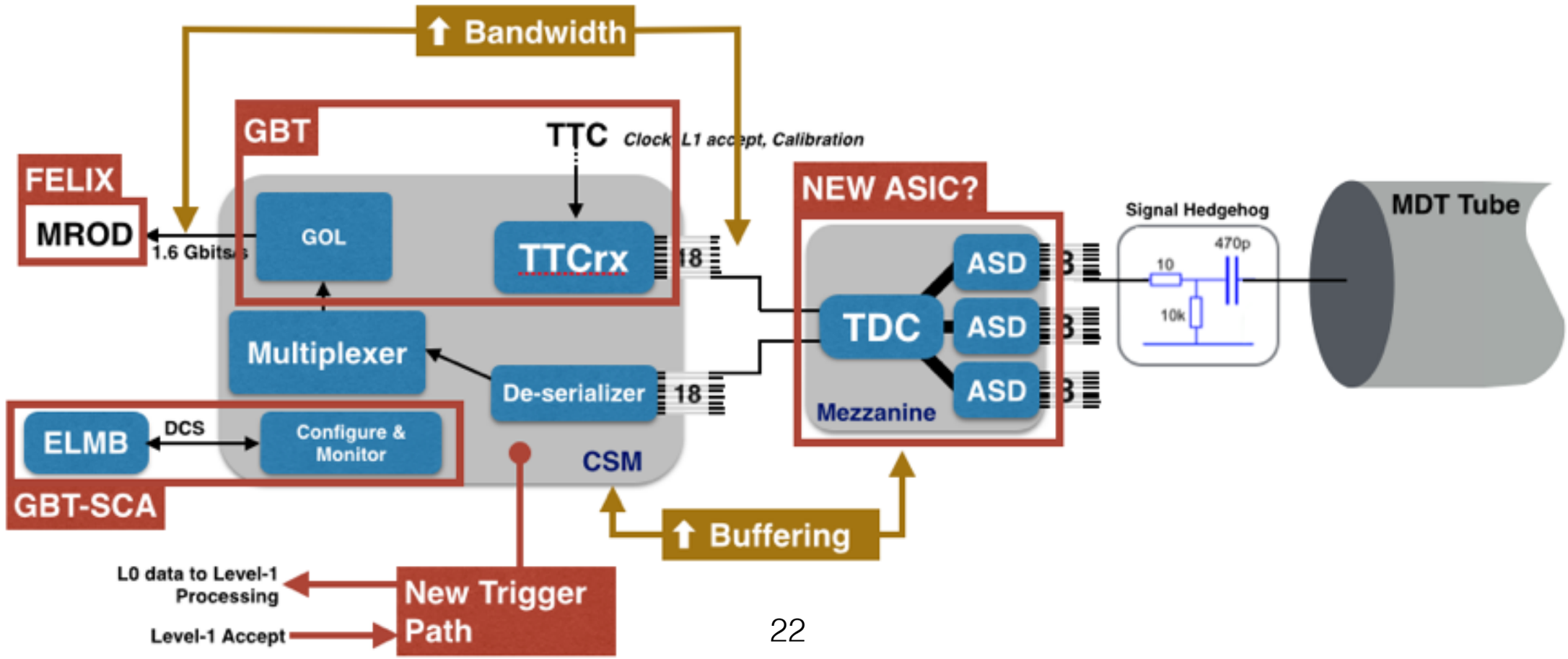


Looking further inside this functional diagram…



Phase II Muon Upgrade

- Higher bandwidth from TDC's to CSM and CSM to USA15 and deeper buffers for mezzanine and CSM to handle the higher rates and longer latencies
- New trigger path - mezzanine sends pre-trigger data to CSM to be passed to USA15 before Level-0 decision decides to use it or not for Level-1 trigger algorithms
- Timing, Trigger, and Control (TTC) and GOL will be replaced by CERN GBT system
- Configure and Monitoring performed by GBT-SCA
- Front-end link exchange system (FELIX) will replace ROD-ROS to perform data collection from CSM



Replacement effort off-site: **Dan Levin**

1. System-wide prep tasks:
   - A. Procurement of cables ..... 1 month
   - B. Design of motherboards ..... 2 month
   - C. Fabrication/procurement of mother boards .... 2 month
   - D. Design/setup test station for MB + cables .... 2 month
   - E. Cable prep ..... 7 person-months
     - (print out labels, sort cables, apply to cables for 15,000 cables 5 min/ cable, cable testing)
     - Can be done with 4 students in parallel process in 6 weeks.
   - F. Mother board + cable pre-assembly .....
     - cable selection , mounting on MB +
     - testing of assembled units = 1/2 hr * 1100 = 3 person-months
     - crating and shipping to CERN 1 week
     - receiving at CERN, storage until installation 1 day

     - ➔ total prep tasks Labor only: 10 person-months

Replacement efforts – in cavern

1. On chamber tasks removal of the old hardware: 30 - 70 min/chamber
   - A. positioning the crane or platform 10 min/chamber
   - B. removal of outer Faraday cage shell 5 min/chamber
   - C. removal of old cables
     - remove fasteners: 15 min/chamber
     - remove ground screws & unplug: 15 min/chamber
     - remove motherboard assembly w/old CSM: 20 min/chamber
     - store in box on crane 5 min./chamber
2. Install new stuff: 7 – 60 min/chamber
   - A. mount new motherboard assembly: 20 min
   - B. plug in power supply line & strain relief: 3 min
   - C. route 16 cables & mount strain relief to each mezzanine: 30 min
   - D. install new mezz cards: 1 min
   - E. re-install outer FC shell: 5 min
   - F. plug in cables: 0.25 min

➔ 40– 130 min/chamber

- mezz card replacement only
- mezz card + cable replacement